

12/29/03

Form PTO-1449 (Modified)		Atty Docket No.: 42P18244		Serial No.: Unknown	
List of Patents and Publications Statement (Use several sheets if necessary)				Applicant: Justin K. Brask et al.	
				Filing Dat : Herewith	

REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS			
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
TL	AA	6,063,698	Tseng et al.	438	585	
	AB	6,184,072	Kaushik et al.	438	197	
	AC	6,420,279	Ono et al.	438	785	
	AD	6,475,874	Xiang et al.	438	396	
	AE	6,514,828	Ahn et al.	438	240	
	AF	6,544,906	Rotondaro et al.	438	785	
	AG	6,617,209	Chau et al.	438	240	
	AH	6,617,210	Chau et al.	438	240	
	AI	US2002/0197790	Kizilyalli et al.	438	240	
	AJ	US2003/032303	Yu et al.	438	770	
TL	AK	US2003/0045080	Visokay et al.	438	591	

FOREIGN PATENT DOCUMENTS							
		Document No.	Date	Country	Class	Sub-Class	Translation
	AL						
	AM						

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
TL	AN	Polishchuk et al. "Dual Workfunction CMOS Gate Technology Based on Metal Interdiffusion," www.eesc.berkeley.edu , 1 page
	AO	Doug Barlage et al., "High-Frequency Response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics", 2001 IEEE, 4 pages.
	AP	Lu et al., "Dual-Metal Gate Technology for Deep-Submicron CMOS Devices", dated April 29, 2003, 1 page.
	AQ	Schwantes et al., "Performance Improvement of Metal Gate CMOS Technologies with Gigabit Feature Sizes", Technical University of Hamburg-Harburg, 5 pages.
	AR	Doczy et al., "Integrating N-type and P-type Metal Gate Transistors", Serial No. 10/327,293, Filed December 20, 2002
	AS	Brask et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/387,303, Filed March 11, 2003
	AT	Brask et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/391,816, Filed March 18, 2003
	AU	Chau et al., "A Method for Making a Semiconductor Device Having a Metal Gate Electrode", Serial No. 10/431,166, Filed May 6, 2003
	AV	Brask et al. "A Selective Etch Process for Making a Semiconductor Device Having a High-K Gate Dielectric," Serial No. 10/652,546, filed August 28, 2003
	AW	Brask et al. "A Method for Making a Semiconductor Device Having a High-K Gate Dielectric," Serial No. 10/642,796, filed August 28, 2003
	AX	Brask, "Methods and Compositions for Selectively Etching Metal Films and Structures," Serial No. 10/658,225, filed September 8, 2003
	AY	Brask et al., "A Method for Making a Semiconductor Device that Includes a Metal Gate Electrode", Serial No. Unknown, Filed December 18, 2003
TL	AZ	Brask et al. "A Method for Making a Semiconductor Device with a Metal Gate Electrode that is Formed on an Annealed High-K Gate Dielectric Layer", Serial No. Unknown, Filed December 19, 2003

Examiner	Date Considered
	02/28/05

(use as many sheets as necessary)

Application Number	10/748,559
Filing Date	December 29, 2003
First Named Inventor:	Justin K. Brask et al.
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	42P18244

Sheet 1 of 1

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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ² Number ⁴ Kind Code ³ (if known)				

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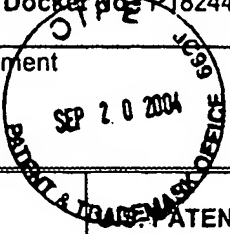
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

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Based on Form PTO/SB/08A (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/10/03.


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REFERENCE DESIGNATION		PATENT DOCUMENTS				
Examiner Initials	Document No.	Class	Sub-Class	Filing date if appropriate		
TL	AA	6,410,376 B1	Ng et al.	438	199	
	AB	6,586,288 B2	Kim et al.	438	183	
	AC	US2002/0058374 A1	Kim et al.	438	228	
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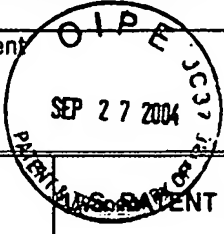
FOREIGN PATENT DOCUMENTS							
Document No.	Date	Country	Class	Sub-Class	Translation		
AP							
AQ							
AR							

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
	AS	
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	AY	
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Examiner 	Date Considered 02/28/05
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TL	AA	6,255,698 B1	Gardner et al.	257	369	
	AB					
	AC					
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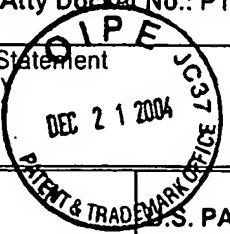
FOREIGN PATENT DOCUMENTS							
Document No.	Date	Country	Class	Sub-Class	Translation		
TL AP EP 0 899 784 AZ	3/3/1999						
TL AQ GB 2 358 737 A	4/24/2001						
AR							

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
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Examiner Initials	Document No.	Class	Sub-Class	Filing date if appropriate		
TZ	AA	6,642,131 B2	Harada	438	591	
	AB	6,667,246 B2	Mitsuhashi et al.	438	756	
	AC					
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